Remarks

Claims 1-11 are pending in the application. Reconsideration and allowance of the application are respectfully requested.

The non-final Office Action dated October 11, 2007 lists the following objection and rejections: claim 7 is objected to due to a grammatical informality; claims 7 and 10 stand rejected under 35 U.S.C. 112(2); claims 1-3 and 6 stand rejected under U.S.C. 102(b) over Wieczorek *et al.* (U.S. Patent No. 6,274,894); claims 4-5 stand rejected under 35 U.S.C. 103(a) over Wieczorek in view of Chau *et al.* (U.S. Patent No. 5,710,450); claims 7-10 stand rejected under U.S.C. 103(a) over Chau in view of Andideh *et al.* (U.S. Patent No. 6,121,100) and further in view of Wieczorek

In response to the objection to claim 7 and to the Section 112(2) rejection of claims 7 and 10, Applicant has made minor amendments to claim 7. Applicant respectfully submits that these amendments render the objection to claim 7 and the Section 112(2) rejection of claims 7 and 10 moot. Thus, Applicant requests that the objection to claim 7 and the Section 112(2) rejection of claims 7 and 10 be withdrawn.

Applicant respectfully traverses the Section 102(b) rejection of claims 1-3 and 6 because the cited portions of the Wieczorek reference do not correspond to the claimed invention which includes, for example, aspects directed to each portion of second semiconductor material extending between the substrate and the spacer substantially as far as a limit coming in line with one side of the gate electrode in the perpendicular direction. The Office Action erroneously asserts that Wieczorek's semiconductor portions 56 correspond to the claimed portions of second semiconductor material. However, the cited portions of Wieczorek teach that trenches 52 are self aligned to sidewalls of encapsulated gate conductor 44 (specifically, to sidewalls of dielectrics 50), and the remaining portions of trenches 52 are filled with portions 56. *See, e.g.,* Figure 7 and 9; Col. 10:52-59 and Col. 12:16-17. As is clearly shown in Wieczorek's Figure 9 (reproduced below with the sidewalls of gate conductor 44 highlighted), semiconductor portions 56 do not extend to the sidewalls of gate conductor 44 as do the portions of second semiconductor material of the claimed invention (*see, e.g.,* Applicant's Figure 1).

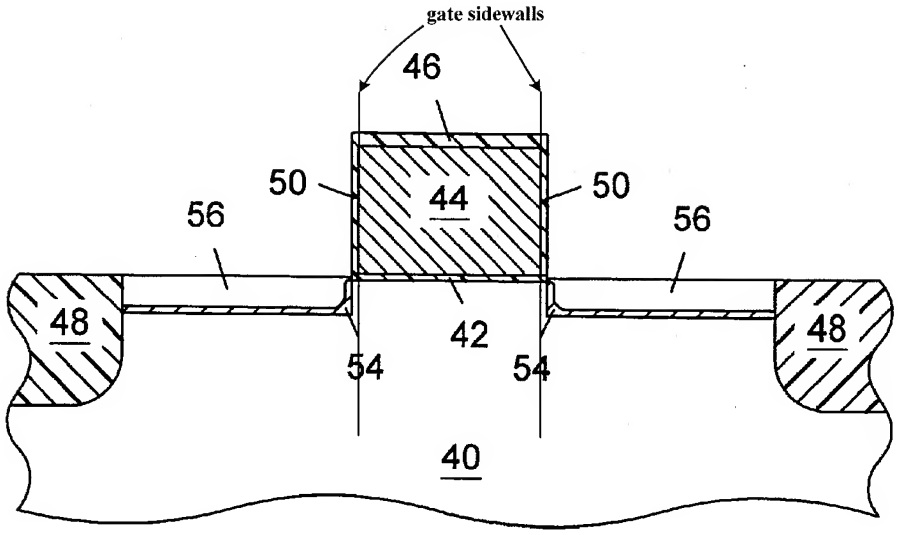


Fig. 9

Instead, Wieczorek's semiconductor portions 56 only extend to the sidewalls of dielectrics 50 since the trenches 52 (in which portions 56 are formed) are self aligned to the sidewalls of dielectrics 50. Therefore, Wieczorek's semiconductor portions 56 do not correspond to the claimed portions of second semiconductor material. Accordingly, the Section 102(b) rejection of claims 1-3 and 6 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the Section 103(a) rejection of claims 4-5 (based upon the Wieczorek reference) because the cited portions of Wieczorek do not correspond to the claimed invention as discussed above in relation to the Section 102(b) rejection of claim 1. In at least this regard, the Section 103(a) rejection of claims 4-5 is improper in that claims 4-5 depend from claim 1. Therefore, Applicant requests that the Section 103(a) rejection of claims 4-5 be withdrawn.

Applicant further traverses the Section 103(a) rejection of claim 5 because the cited portions of the Chau reference do not correspond to aspects of the claimed invention directed to each encapsulation portion extending between the spacer and the portion of second semiconductor material above which said encapsulation portions is deposited. The Office Action erroneously asserts that Chau's second semiconductor material 420 corresponds to the claimed encapsulation portions. However, as is clearly shown by Chau in Figure 4, Chau's second semiconductor material 420 does not extend between semiconductor material 314 and sidewall spacer 318. Thus, Chau's second semiconductor material 420 does not correspond to the encapsulation portions of the

claimed invention. Accordingly, the Section 103(a) rejection of claim 5 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the Section 103(a) rejection of claims 7-10 because the cited portions of the Chau reference do not correspond to the claimed invention which includes, for example, aspects directed to removing two lateral parts of the first semiconductor material with each lateral part extending between the substrate and the spacer up to the opposite sides of the gate electrode. As is clearly shown by Chau in Figure 3B, the recesses 312 formed by Chau in substrate 300 do not extend between substrate 300 and spacers 310 and the recesses 312 also do not extend up to the sidewalls of gate electrode 306. Thus, the cited portions of the Chau reference do not correspond to the claimed invention. Accordingly, the Section 103(a) rejection of claims 7-10 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the Section 103(a) rejection of claims 7-10 because the cited portions of the Andideh reference do not correspond to the claimed invention which includes, for example, aspects directed to in each lateral part, forming a portion of a second semiconductor material that extends up to the opposite sides of the gate electrode. As is clearly shown by Andideh in Figure 3B, semiconductor material 318 does not extend up to the sidewalls of gate electrode 306; instead Andideh teaches that semiconductor material 318 only extends up to spacer 314 which is formed along the sidewalls of gate electrode 306. Thus, the cited portions of the Andideh reference do not correspond to the claimed invention. Accordingly, the Section 103(a) rejection of claims 7-10 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the Section 103(a) rejection of claims 7-10 because the cited portions of the Wieczorek reference do not correspond to the claimed invention which includes, for example, aspects directed to heating the portions of second semiconductor material to a temperature that is between the melting points of the first and second semiconductor materials. The cited portions of Wieczorek simply teach that an anneal is performed. *See, e.g.,* Col. 13:20-45. However, these portions of Wieczorek fail to make any mention of the temperature at which the annealing is performed, much less that it is performed at a temperature that is between the melting points of first and second semiconductor materials as in the claimed invention. Thus, the cited portions of the

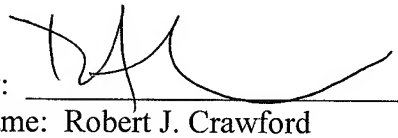
Wieczorek reference do not correspond to the claimed invention. Accordingly, the Section 103(a) rejection of claims 7-10 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: 
Name: Robert J. Crawford
Reg. No.: 32,122
651-686-6633
(NXPS.390PA)